MSE SEMINAR

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113 McBryde Hall
3:30 – 4:30 PM
Refreshments at 3:00 PM

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Electrical Characterization and Reliability of Electron Device Instability

ABSTRACT

As we venture into the "Internet of Things" (IoT) era, "conventional" semiconductor device dimensions continue to reduce along with reduced margins (i.e., ranges) in specifications. Furthermore, new device designs and materials are being investigated to meet future IoT demands because conventional silicon technology cannot fulfill all of the requirements for low-cost manufacturing with the necessary performance requirements and/or reliability. As new materials or device architectures are introduced, electrical characterization is ultimately required to corroborate and/or link "physical" characterization findings. In addition, coupling test results with physical characterization can lead to fundamental understanding of the origin of the improvements – or lack thereof – when investigating the performance or reliability of devices. Also, electrical testing can help explain the instability in specifications such as threshold voltage (V_t) instability – both "time zero" and time dependent mechanisms. General instability in devices can become a significant problem in highly scaled devices because one unwanted charge (i.e., a trapped electron) could significantly impact performance and reliability. Therefore, proper electrical characterization methodology development while also having robust, but simple test structures is critical to fundamental understanding device behavior.

In this work, our research group will demonstrate how we use advanced electrical characterization methodologies and/or appropriate test structures to facilitate the preliminary understanding of fundamental mechanisms of the particular instability or performance metric under investigation. In one study, we investigate the significant V_t instability in zinc oxide (ZnO) thin-film transistors with hafnium oxide gate dielectrics where we demonstrate irreversible bulk electron trapping – contrary to what is typically seen in Hf-based dielectrics on conventional silicon transistors. In another investigation, we developed a simple, dual-gate test structure to investigate dielectric interfaces and metal contacts with transition metal dichalcogenides (TMD) – specifically MoS_2 – as the semiconducting substrate. The initial electrical characterization results show that the test structure is able to help correlate physical characterization results of an interface treatment that provided the proper insight into materials and fabrication processes that ultimately impact device performance.

BIOSKETCH

Chadwin D. Young received his B.S. degree in Electrical Engineering from the Univ. of Texas at Austin in 1996 and his M.S. and Ph.D. in EE from the North Carolina State University in 1998 and 2004, respectively. In 2001, he joined SEMATECH where he completed his dissertation research on high-k gate stacks and continued this research at SEMATECH as a Senior Member of the Technical Staff working on electrical characterization and reliability methodologies for the evaluation of high-k gate stacks on current and future device architectures. He joined (09/12) the Materials Science and Engineering Department at the University of Texas at Dallas as an Assistant Professor where his research focus is on electrical characterization and reliability methodologies for the evaluation of future materials and devices. He has authored or co-authored 250+ journal and conference papers. He has served: on the management or technical program committees of IIRW, IRPS, SISC, IEDM, WoDiM; as Guest Editor for IEEE Transactions on Device and Materials Reliability; and as a peer reviewer for several journals. He is currently a Senior Member of IEEE.